IN THE SPECIFICATION

The paragraph beginning at page 1, line 4 is amended as follows:

Cross Reference To Related Applications

This application is related to the following co-pending, commonly assigned U.S. patent applications: "DRAM Cells with Repressed Memory Metal Oxide Tunnel Insulators," attorney docket no. 1303.019US1, ~~serial number~~ serial number 09/945,395, "Programmable Array Logic or Memory Devices with Asymmetrical Tunnel Barriers," attorney docket no. 1303.020US1, ~~serial number~~ serial number 09/943,134, "Dynamic Electrically Alterable Programmable Memory with Insulating Metal Oxide Interpoly Insulators," attorney docket no. 1303.024US1, ~~serial number~~ serial number 09/945,498, and "Flash Memory with Low Tunnel Barrier Interpoly Insulators," attorney docket no. 1303.014US1, ~~serial number~~ serial number 09/945,507, "SRAM Cells with Repressed Floating Gate Memory, Metal Oxide Tunnel Interpoly Insulators," attorney docket no. 1303.028US1, ~~serial number~~ serial number 09/945,554, "Programmable Memory Address and Decode Devices with Low Tunnel Barrier Interpoly Insulators," attorney docket no. 1303.029, ~~serial number~~ serial number 09/945,500, which are filed on even date herewith and each of which disclosure is herein incorporated by reference.

Please amend the paragraph beginning at page 6, line 15, as follows

Additionally, graded composition insulators to increase the tunneling probability and reduce erase time have been described by the same inventors. (See, L. Forbes and J. M. Eldridge, "GRADED COMPOSITION GATE INSULATORS TO REDUCE TUNNELING BARRIERS IN FLASH MEMORY DEVICES," application serial no. 09/945,514 ~~no.~~).